**Amendments to the Claims**

No amendments have been made to the claims. This listing of the claims is provided for the Examiner's convenience.

**Listing of Claims:**

1. (Previously presented) In an apparatus having a bus operatively coupled to a first controller chip and a first channel chip, the channel chip having several registers, the apparatus also having a storage medium operatively coupled to the bus through a storage medium interface, a method for retrieving data recorded on the storage medium comprising steps of:

(a) retrieving a first portion of the recorded data via the bus;

(b) updating some of the registers via the bus; and

(c) retrieving a second portion of the recorded data via the bus.

2. (Original) The method of claim 1 in which the interface includes a read head, further comprising a step (d) of repositioning the storage medium interface with respect to the storage medium, between retrieving steps (a) and (c).

3. (Original) The method of claim 2 in which the interface has a plurality of operating parameters that are modified in updating step (b).

4. (Previously presented) The method of claim 1 in which the registers contain at least one read channel parameter value selected from the group consisting of: a precompensation value, a filter coefficient value, and a phase offset value.

5. (Previously presented) The method of claim 1 in which the registers contain at least one mode-indicative value.

6. (Original) In a storage system having a disc with at least two zones having zone identifiers $Z_A$ and $Z_B$, an interface configured to read data in zone $Z_A$, a target segment in zone $Z_B$, a value table indexed by zone identifiers, a direct memory access (DMA) controller, a microprocessor coupled to the DMA controller, and several read channel registers each containing a value, a method comprising steps of:

(a) retrieving via the DMA controller several values indexed by zone identifier $Z_B$;

(b) updating at least some of the read channel register values from the retrieved values;

(c) reconfiguring the interface to read data in zone $Z_B$; and

(d) reading the target segment.

7. (Original) The method of claim 6 in which the target segment has a predetermined starting track number, further comprising a step of deriving zone identifier $Z_B$ from the predetermined starting track number before retrieving step (a).

8. (Original) The method of claim 6 in which the interface includes at least one head, in which positioning step (c) includes a step of (c1) moving the at least one head radially across the disc, the moving step (c1) beginning before retrieving step (a) is complete.

9. (Original) The method of claim 8 in which moving step (c1) begins before retrieving step (a) begins.

10. (Original) The method of claim 6 in which zone $Z_B$ has a corresponding data rate $R_B$ that is not in common with zone $Z_A$, in which positioning step (c) includes a step of (c2) sampling a signal from the interface at an initial frequency that is an integer multiple of data rate $R_B$.

11. (Original) The method of claim 6 further comprising prior steps of:

(e) configuring the interface to read data in zone $Z_B$;

(f) receiving a signal from the interface;

(g) deriving several values indicative of the interface's performance in zone $Z_B$ from the received signal; and

(h) storing some of the derived values in the value table each at a position associated with zone $Z_B$.

12. (Original) The method of claim 6 in which the storage system includes an integrated circuit comprising the microprocessor, and in which the retrieving step (a) comprises issuing at least one but fewer than 10 commands from the microprocessor to the DMA controller.

13. (Original) The method of claim 12 further comprising steps of:

(j) sensing position data from a servo sector via the interface; and

(k) deriving a servo control signal from the sensed position data with the microprocessor during step (b).

14. (Original) The storage system of claim 6 configured to perform the method of claim 6 further comprising a printed circuit board assembly including a memory containing the value table, the storage system comprising:

a master integrated circuit (IC) containing the microprocessor and the direct memory access (DMA) controller, the DMA controller being operatively coupled to the memory;

a slave IC containing the several read channel registers; and

a bus coupled between the master IC and the slave IC, the bus controllable by the DMA controller to perform updating step (b).

15. (Previously presented) An apparatus comprising:

an interface configured to read data from a storage medium;

a memory containing several values indexed by zone identifiers;

a first controller chip containing a microprocessor and a direct memory access (DMA) controller, the DMA controller operatively coupled to the memory;

a first channel chip having several registers; and

a bus operatively coupled between the interface and the chips, the bus controllable by the DMA controller to read from the memory and to update several of the registers in response to a zone transition event.

16. (Previously presented) A method comprising steps of:

(a) providing data via a bus;

(b) updating at least one register or parameter via the bus; and

(c) providing data via the bus responsive to the updating.

17. (Previously presented) The method of claim 16 wherein the bus is serial.

18. (Previously presented). The method of claim 16 wherein the bus is parallel.

19. (Previously presented) The method of claim 16 wherein the steps are controlled by a processor.

20. (Previously presented) The method of claim 16 wherein the steps are controlled by a direct memory access apparatus.

21. (Previously presented) A method for reducing processing burden on a processing device, comprising steps of transmitting first data via a bus coupled to the processing device, updating at least one register or parameter via the bus, and transmitting second data via the bus in response to the updating step.

22. (Previously presented) The method of claim 21 wherein the bus is characterized as a selected one of a serial bus or a parallel bus.

23. (Previously presented) The method of claim 21 wherein the first and second data are respectively characterized as user data transferred between a host device and a storage medium.

24. (Previously presented) The method of claim 23, wherein the user data are transmitted via the bus between a read/write channel and a controller.

25. (Previously presented) The method of claim 21, wherein the first data are transmitted at a first data rate and the second data are transmitted at a second rate different than the first rate.